

# Classical Simulations of Large-Scale Quantum Computers

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ASCR Workshop on Quantum Computing for Science  
Topic I: Models of Quantum Computation

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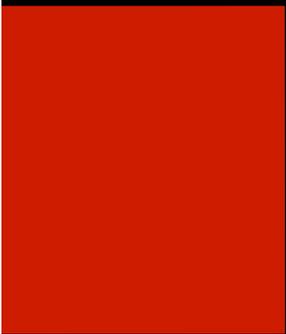
submitted with **Stephan Haas** and **Daniel Lidar**



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# Outline

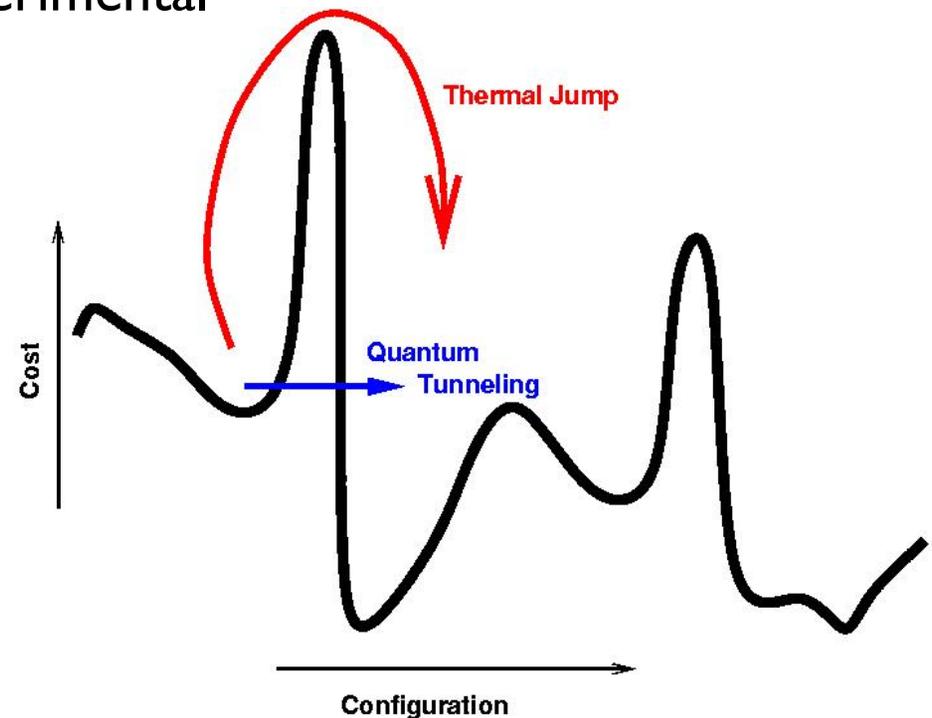
- ❑ importance of characterizing experimental quantum devices
- ❑ example: “classicality” of quantum annealers
- ❑ need for classical simulations



# Characterizing experimental quantum devices

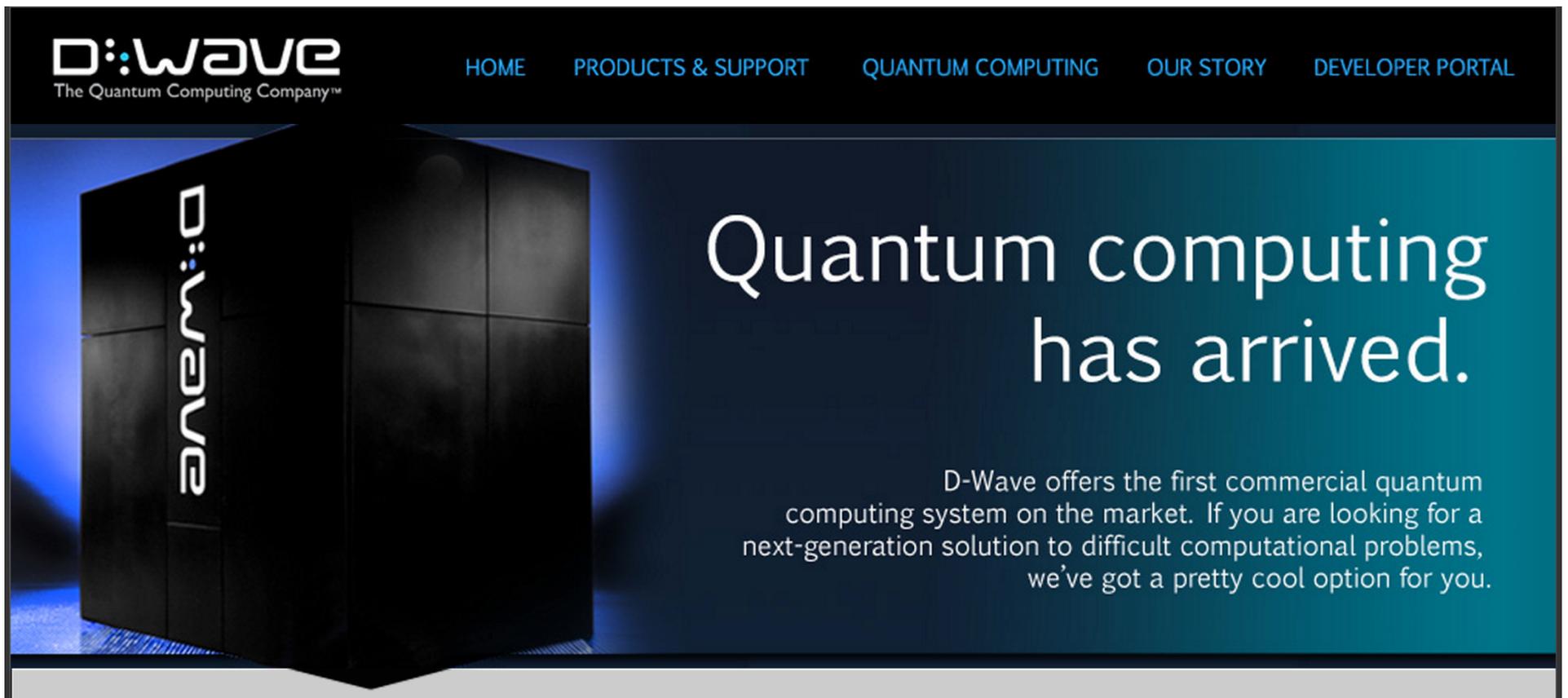
# Introduction

- ❑ **quantum annealing (QA):** an optimization technique based on gradually reducing the magnitude of quantum fluctuations to find global minima, presumably uses quantum tunneling to traverse energy barriers.
- ❑ but...neither theoretical nor experimental evidence of superiority of quantum annealers over thermal annealers (or over other classical methods).
- ❑ **reason is: we do not understand QA well enough to exploit it.**



# Introduction

□ in 2011, D-Wave Systems Inc. have declared:

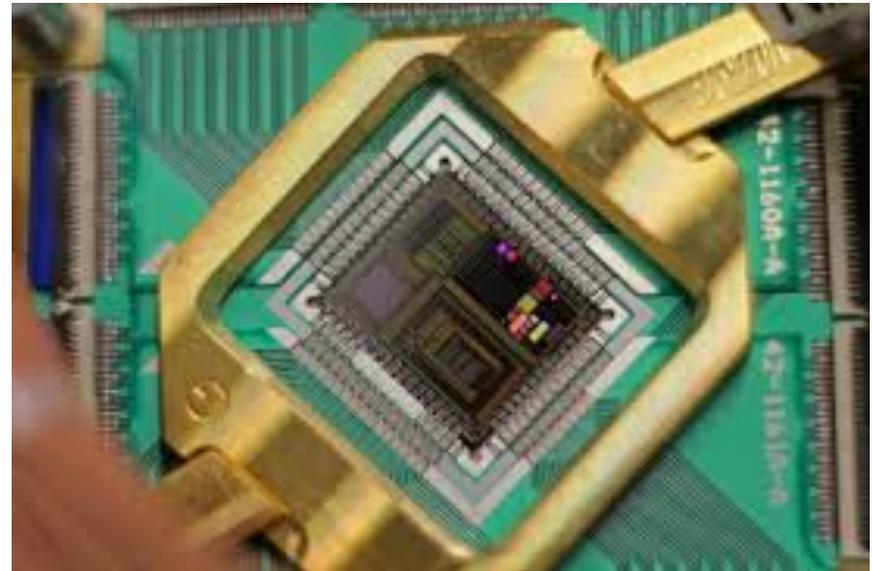


□ but has it?

# The D-Wave Two Chip

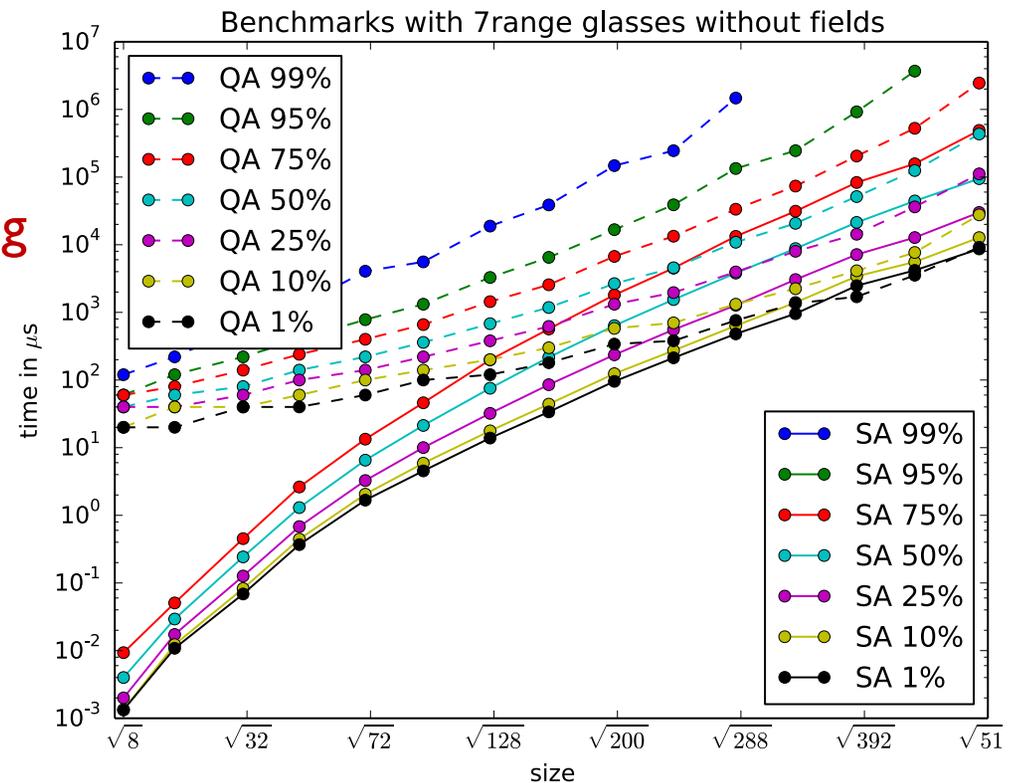
- dealing with the machine has taught us a lot.
- raised **fundamental questions** that extend far beyond the D-Wave chips, e.g., how do we perform proper benchmarking on non-universal devices?
- how do we characterize the “quantumness” or “classicality” of a device?
- are “classically-hard” problems always “quantum-hard”? how do we find counter-examples?

these questions  
will be valid for any near-  
future quantum device



# Benchmarking

- benchmarking tests have been inconclusive so far.
- random MAX 2-SAT instances on the Chimera:
  - S. Santra et al., “MAX 2-SAT with up to 108 qubits” (New J. Phys., 2014).
- random Ising models (no fields  $h_i = 0, J_{ij} = \pm 1$  or similar):
  - S. Boixo, et al., “Quantum Annealing With More Than One Hundred Qubits”, (Nature Phys., 2014).
  - T. F. Rønnow et al., “Defining and detecting quantum speedup”., (Science, 2014).
- no evidence for speedup so far.



# Benchmarking

- the usefulness of quantum annealers depends on the answers to the following two questions:

is “classically-hard” different  
from “quantum-hard?”

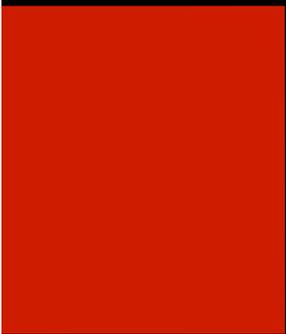
can this difference be detected by  
the annealer in question?

- need to find hard instances (and if possible, find a way to design such).
- can we find a “good parameter” for measuring classical hardness?

# Characterizing quantum devices

when quantum devices become  
“commercially” available, they will need to be  
properly benchmarked and characterized

- ❑ these devices will be non-universal, limited, noisy, prone to errors.
- ❑ some features will be beyond the control of the end user.
- ❑ **how do we do that?**



**Example:**  
**“classicality” of quantum annealers**

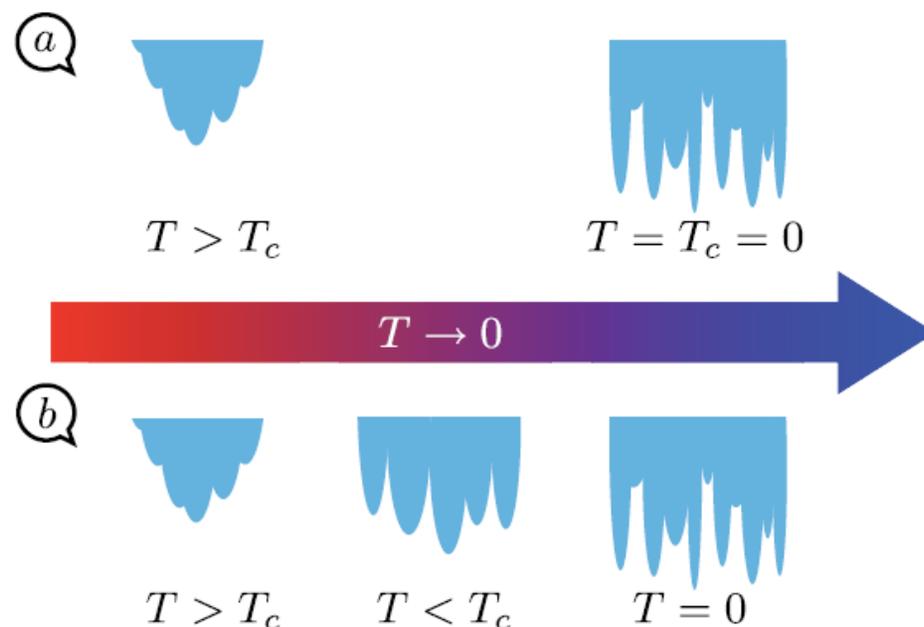
# Generating hard problems

- concrete example:

how “classical” is the D-Wave  
putative quantum annealing chip?

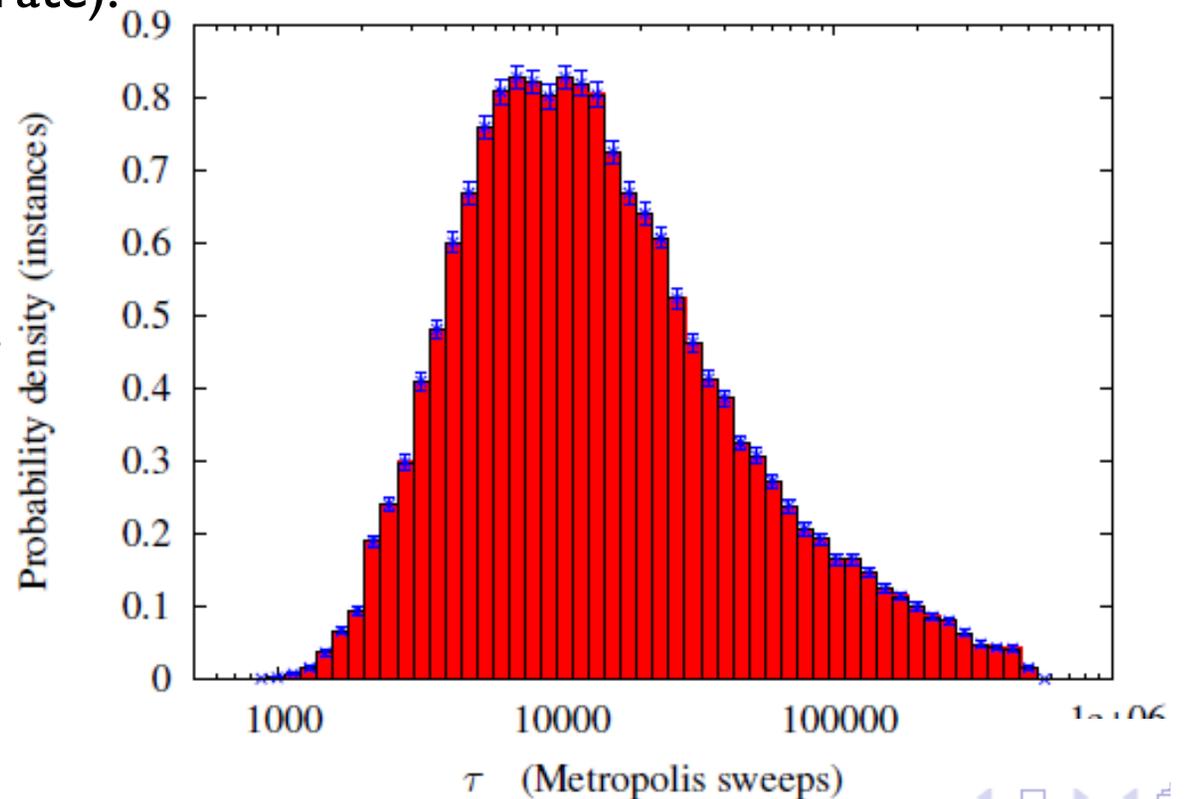
- interesting behavior is expected to emerge when queried with hard problems (Katzgraber et al., 2014).

- can we and how do we generate classically-hard problems?



# Generating hard problems

- by generating millions of instances, and analyzing each by parallel tempering (PT), we assign each instance its own “classical hardness” (the time it takes PT to equilibrate).
- the classical hardness is the average mixing time  $\tau$  (on the temperature grid) of the PT for the instance.
- we get 5 different orders of magnitude of classical hardness.



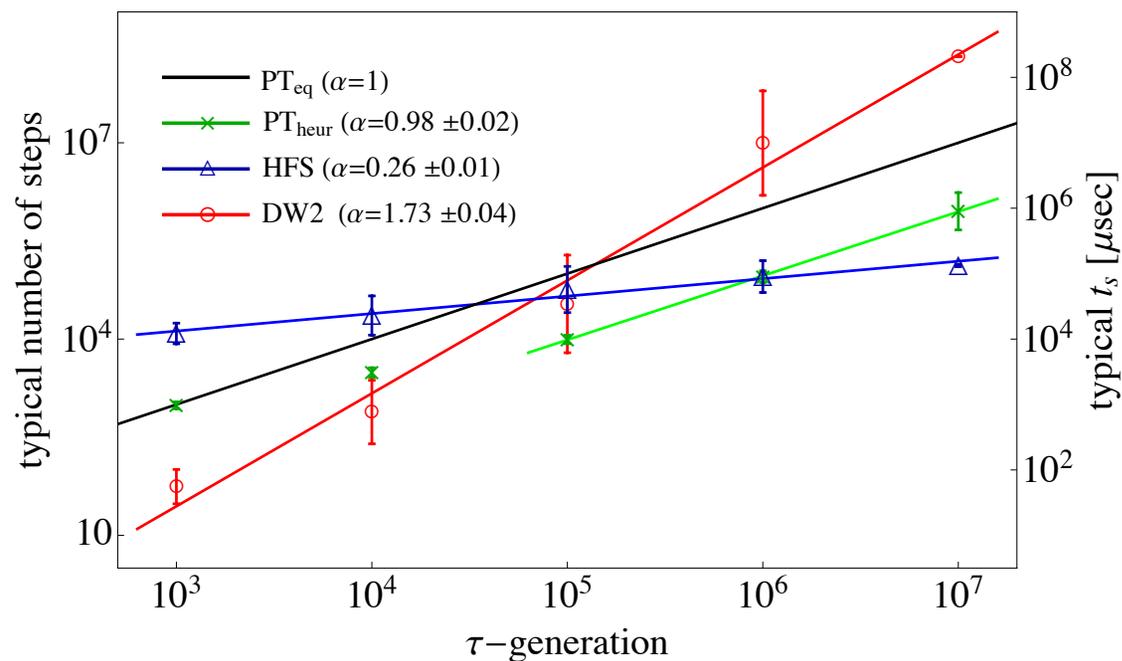
# Chip behavior

- meaningful algorithmic classification at fixed  $N$ :  $\tau$ -scaling.
- parallel tempering: time to solution (tts)  $\sim \tau^1$  (by definition),
- Selby's heuristic (2D-like):  $tts \sim \tau^{\approx 0.3}$  (much better than PT).
- D-wave:  $tts \sim \tau^{1.75}$

- however, not yet schedule-optimized

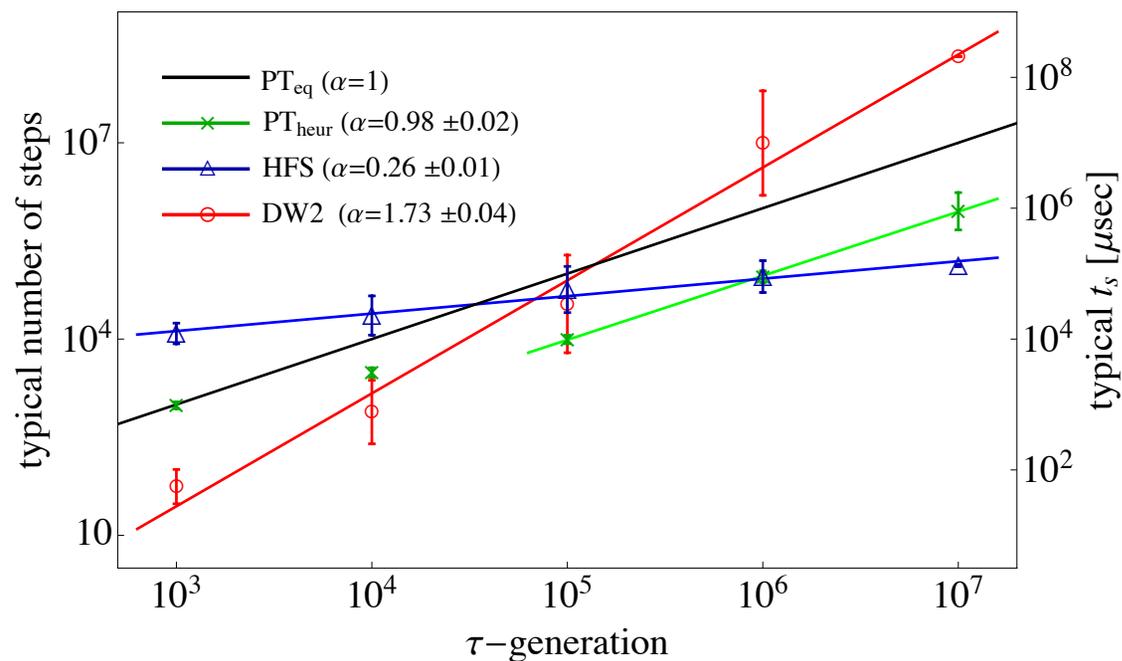
- worse than PT!

- why? Important to understand.



# Resolving performance issues

- this needs to be investigated, could be for several reasons:
- temperature may still be too high.
- programming errors in the  $J$  values may have devastating effects.





need for classical simulations

# need for classical simulations

- ❑ we need to understand what causes the chip's apparent behavior.
- ❑ but we have almost no control over the “knobs” of the chip.
- ❑ experimental testing of different scenarios will take years.
- ❑ the need arises for faithful simulations that would allow us to consider different scenarios and modifications to the device,
- ❑ would also allow us to understand the driving mechanism underlying quantum annealers.
- ❑ understanding the effects of noise (encoding errors) and temperature on the performance.
- ❑ would help to bring forth the quantum signatures of the device.

***Thank You!***

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