Device and Emerging Technologies WG

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- **Metrics for interconnect technologies**
  - Cost/bit/sec
  - Energy/bit
  - Density (bits/sec, per chip, etc.)

Interconnect domains

- On-chip global (cm)
- On-module (cm)
- On board (20cm)
- Intra-cabinet (0.5-1m)
- Inter-cabinet (2-50m)

WG Plan: examine key emerging technologies at multiple domains, evaluate challenges, impact

Key Emerging Technologies

- **CMOS – aggressive scaling as benchmark**

- **Silicon Photonics**
- **Proximity Communications**
  - > Capacitive, inductive
- **MEMS**
- **3-D integration**

- **Speculative: RF, free-space optics, CNTs**

Electrical Signaling Near-term Potentials

- On-chip (cm) ~1 pJ/bit, 100 Tb/s
- On-module (cm) ~2-5 pJ/bit, 1-10 Tb/s per chip
- On board (20cm) ~5-10 pJ/bit, 1-5 Tb/s per module
- Intra-cabinet (0.5-1m) ~10-15 pJ/bit, 1-5 Tb/s per board
- Inter-cabinet (2-50m) ~20-30 pJ/bit, 5-10 Tb/s per cabinet (optical)

- 1pJ → 1MW @ EB/s

Challenges of Silicon Photonics

- **Device-Level**
  - Novel WDM devices, switches, modulators, receivers
  - Integration density
  - low optical loss
  - Thermal stability
  - manufacturability
- **Circuit-Level**
  - Analog circuits in scaled CMOS (voltage headroom, variations,etc.)
  - reliability
  - Energy
  - E/O interface
- **System-Level**
  - Optical packaging
  - Connectors
  - Chip-scale packaging (photonics/electronics)
  - reliability

Critical Off-chip Boundaries

- **Intra-node processor-memory interface**
- **Inter-node**

Maturity/impact/cost

	Maturity			Impact/Rewards			NRE (cost)		
Technical	**High**	**Med**	**Low**	**High**	**Med**	**Low**	**High**	**Med**	**Low**
Intra-node processor-memory interface									
CMOS photonics			x	x			x		
3-D stacking (parallel and orthogonal)		x		x				x	
proximity Comm.		x		x				x	
Inter-node									
dense integrated-photonics to fiber interface		x		x				x	
CMOS photonics			x	x			x		
Packaging (E&O)		x		x			x		
Switching									
optical switching		x			x		x		
MEMS	x				x				x
hybrid (electrical/optical)		x		?	x			x	