Future disruptions in interconnect technology

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- David Miller (Stanford)
- Eby Friedman (U. Rochester)
- Krste Asanovic (Berkeley)
- Uzi Vishkin (U. Maryland)

Nanoscale Silicon Photonics for Interconnection Networks

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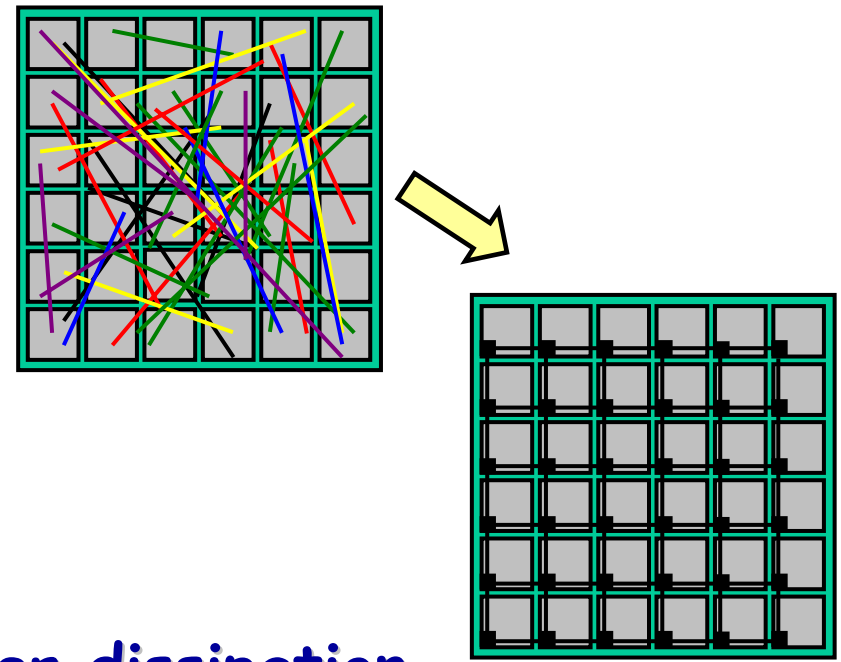
COLUMBIA UNIVERSITY

Global Communications On-Chip

- Growing number of cores: Networks-on-Chip (NoC)
- Shared, packet-switched, optimized for communications
  - Resource efficiency
  - Design simplicity
  - IP reusability
  - High performance



- But… no true relief in **power dissipation**
- **IBM Cell ~30-50% of chip power budget In global interconnect**

Off-chip bandwidth and memory interface

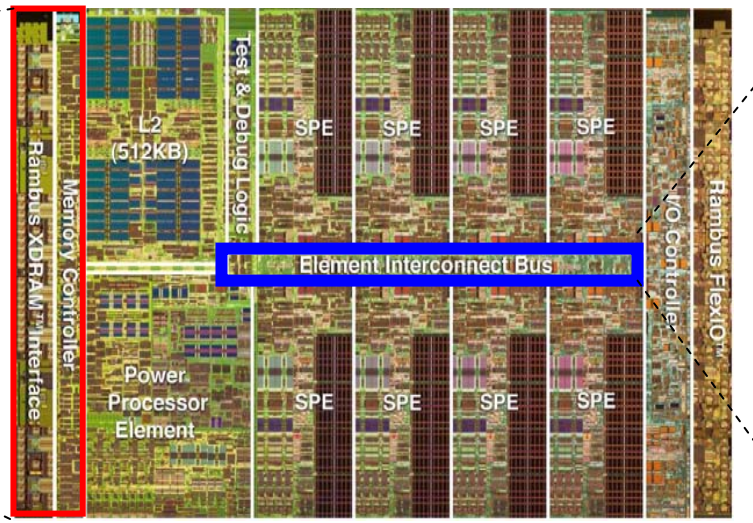
- CMPs are driving massive on-chip interconnect bandwidth and increased need for off-chip communications. Some examples:

Processor	Vendor	Release year	Off-chip bandwidth
Cell Broadband Engine [34]	IBM, Sony, Toshiba	2006	50.6 GBytes/s
Montecito [57]	Intel	2005	10.66 GBytes/s
Niagara [43]	Sun	2003	> 20 GBytes/s
Opteron [38]	AMD	2003	24.5 GBytes/s[1]
GEFORCE 6800[2] [59]	Nvidia	2005	35.2 GBytes/s

Increasing signaling rates, pin counts

Dual Channel Rambus XDR DRAM memory delivers:
12.8GB/s per 32-bit channel

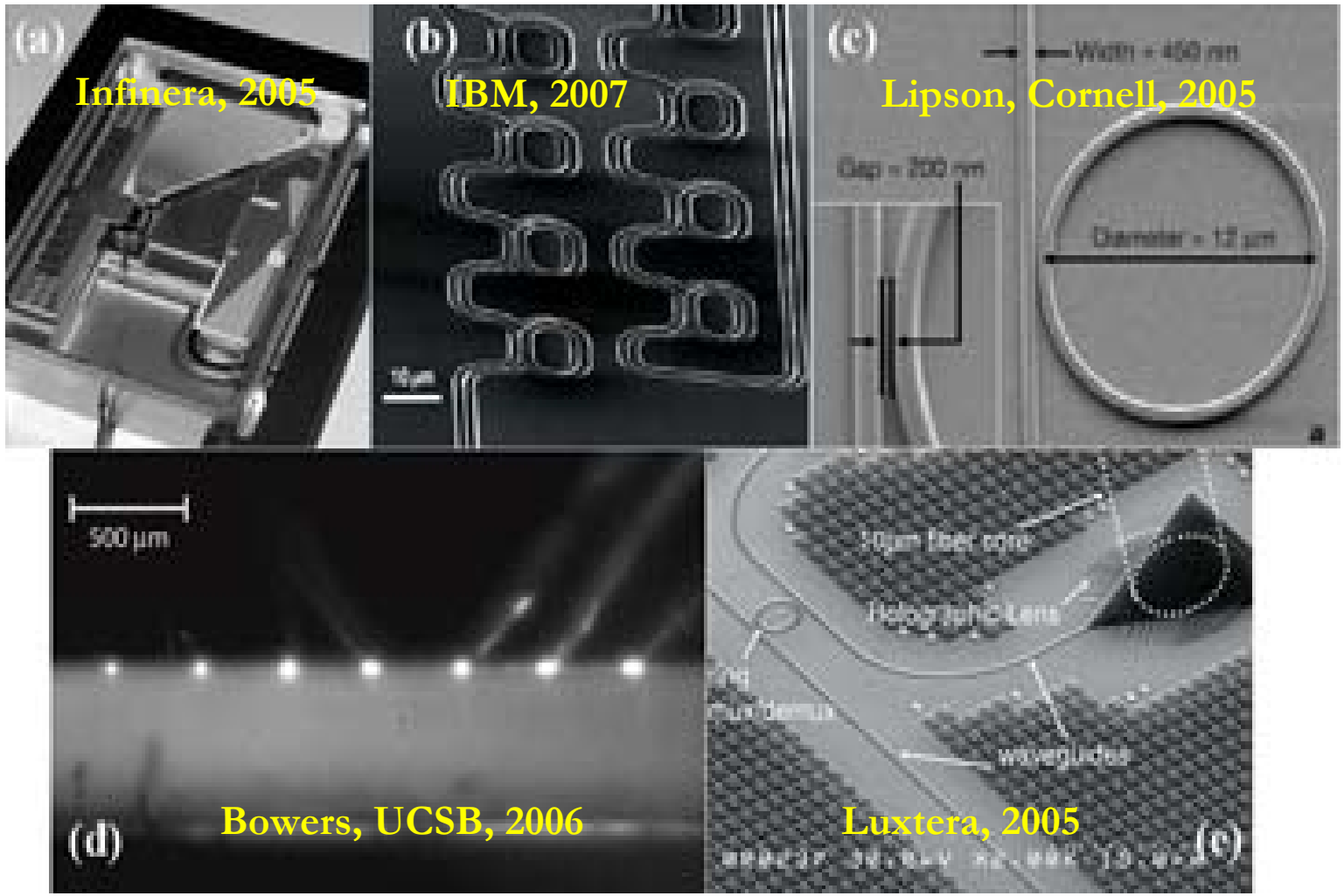
25.6GB/s @3.2Gbit/sec



internal fabric of the chip delivers nearly an order of magnitude more bandwidth:

96 byte per cycle, or 128GB/s

Nanoscale Photonic Integration



Why Photonics?

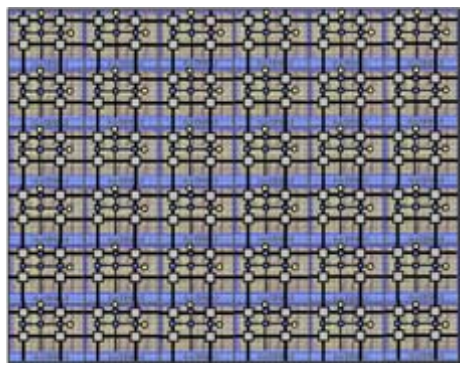
Photonics changes the rules for Bandwidth-per-Watt

OPTICS:

- Modulate/receive ultra-high bandwidth data stream **once** per communication event
- Transparency: broadband switch routes entire multi-wavelength high BW stream
- Low power switch fabric, scalable

ELECTRONICS:

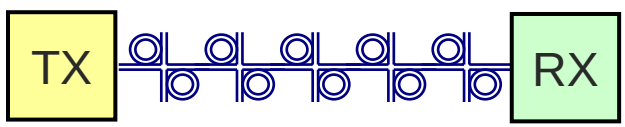
- Buffer, receive and re-transmit at **every switch**
- **Off chip** is pin-limited and really power hungry

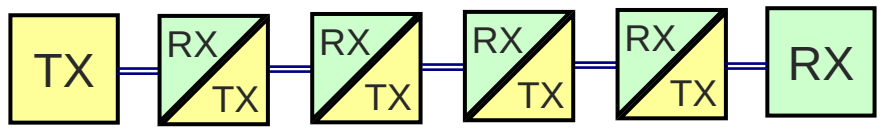


Off-chip BW = On-chip BW for nearly same power

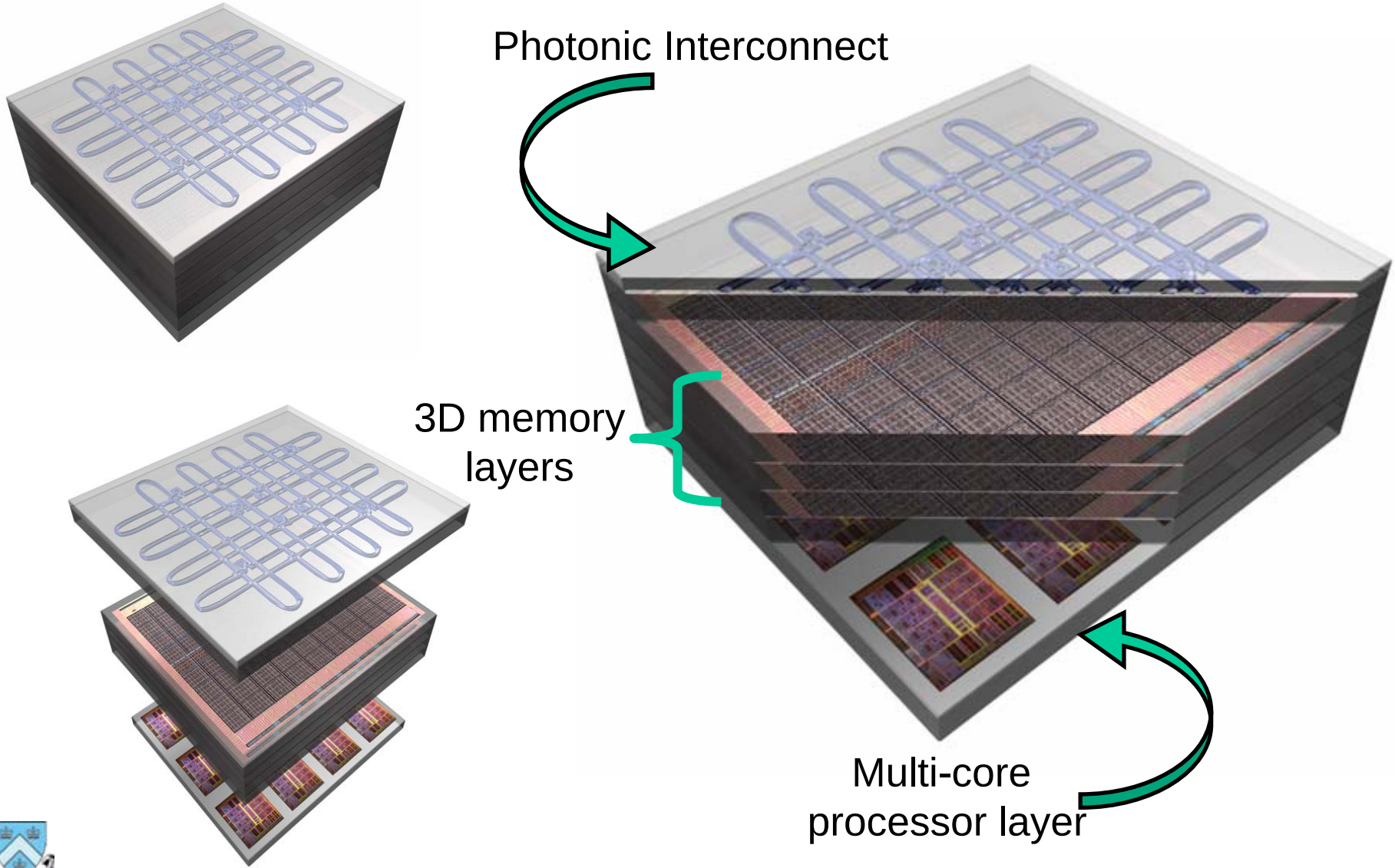
Inter-node and optics to memory possible path to:

balanced, power efficient, scalable BW, low latency computing system





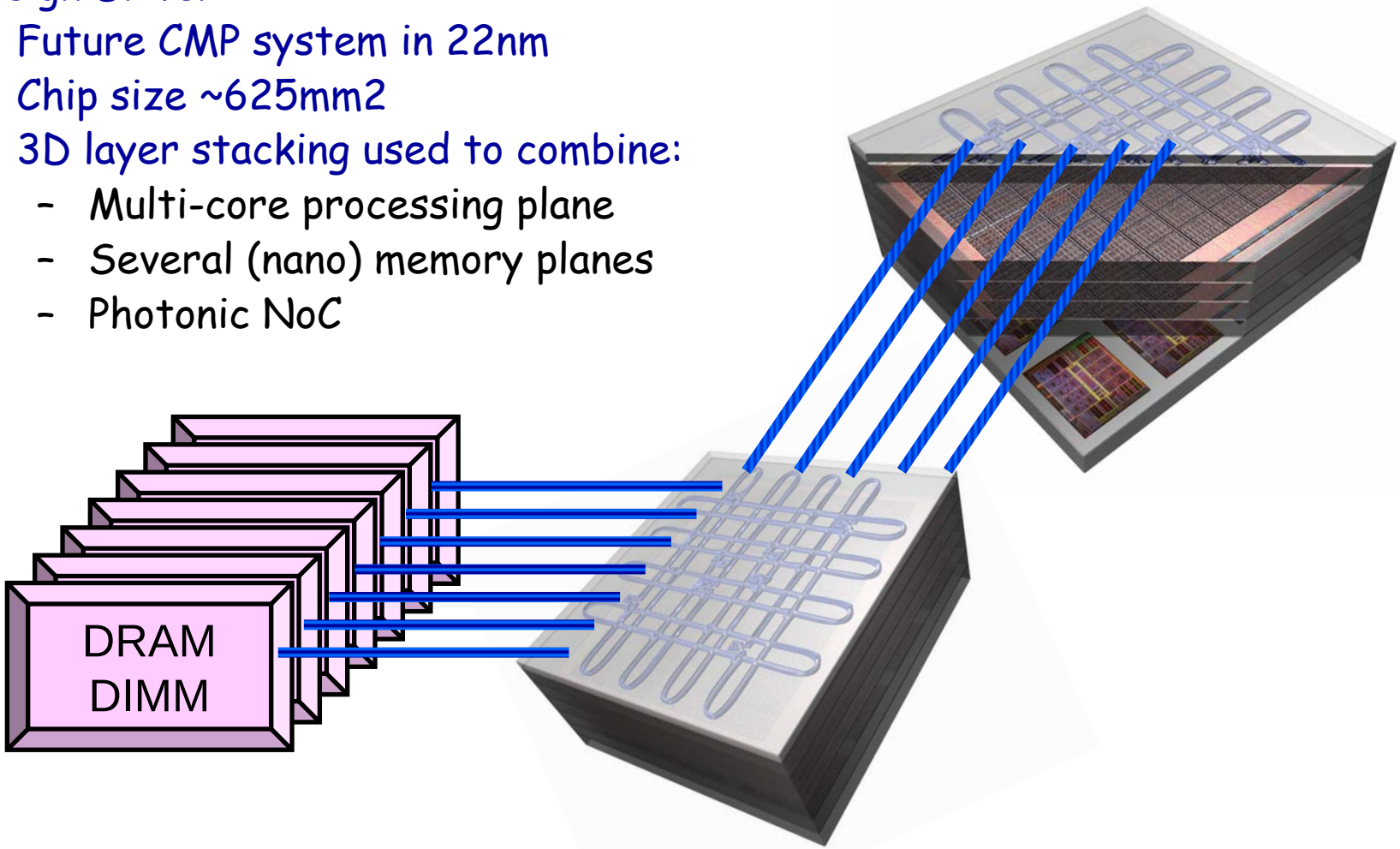
Nanophotonic Interconnected Design Driver



Nanophotonic Interconnected System Concept

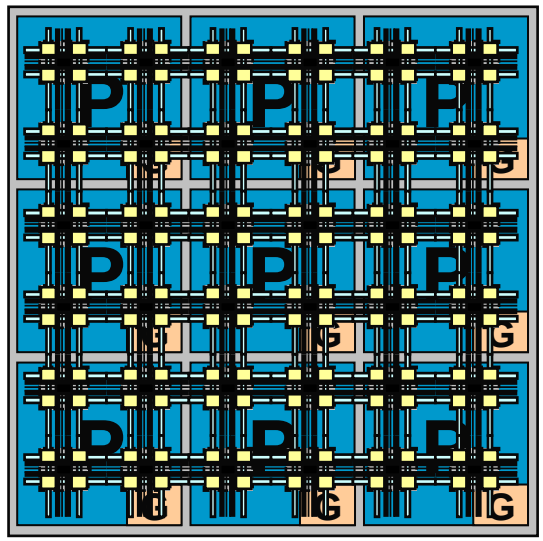
Design Driver

- Future CMP system in 22nm
- Chip size ~625mm2
- 3D layer stacking used to combine:
  - Multi-core processing plane
  - Several (nano) memory planes
  - Photonic NoC

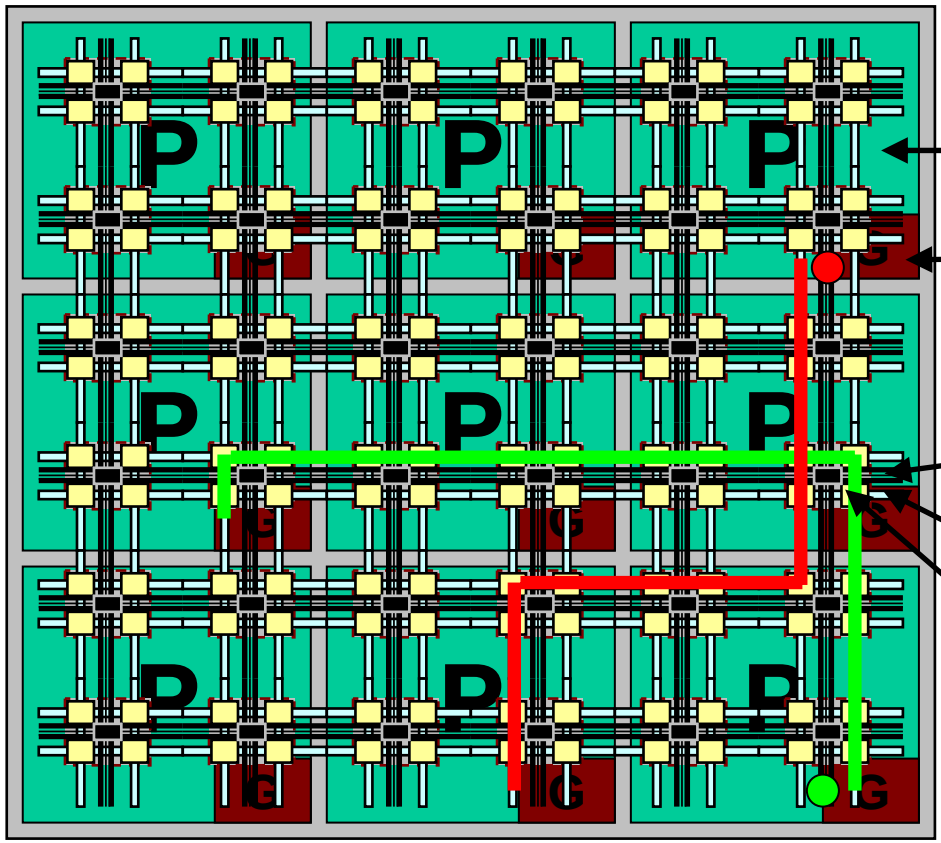


Photonic On-Chip Network

- **Goal: Design a NoC for a chip multiprocessor (CMP)**
- Electronics
  - ✓ Integration density → abundant buffering and processing
  - × Power dissipation grows with data rate
- Photonics
  - ✓ Low loss, large bandwidth, bit-rate transparency
  - × Limited processing, no buffers
- Our solution – a hybrid approach
  - Data transmission in a photonic network
  - Control in an electronic network
  - Paths reserved before transmission → No optical buffering



On-Chip Optical Network Architecture Bufferless, Deflection-switch based



Cell Core
(on processor plane)

Gateway to Photonic NoC
(on processor and photonic planes)

Thin Electrical Control Network
(~1% BW, small messages)

Photonic NoC

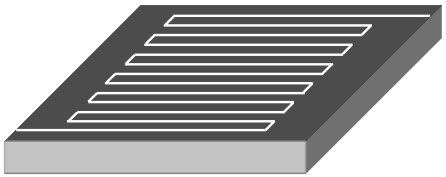
Deflection Switch

DARPA phase I ICON project

Key Building Blocks

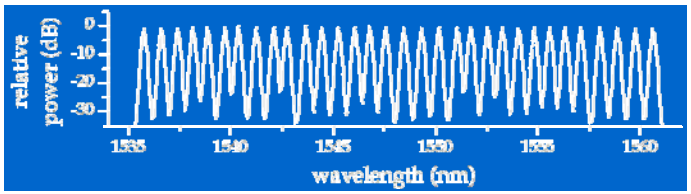
LOW LOSS BROADBAND NANO-WIRES

5cm SOI nanowire



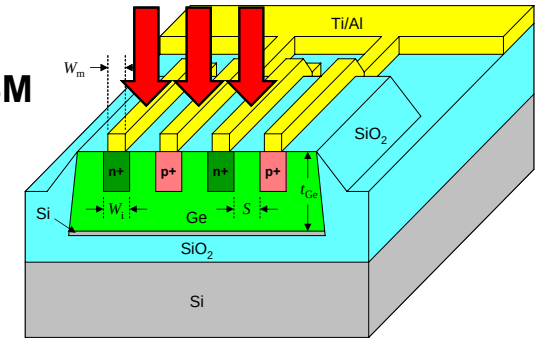
IBM/Columbia

1.28Tb/s (32 λ x 40Gb/s)



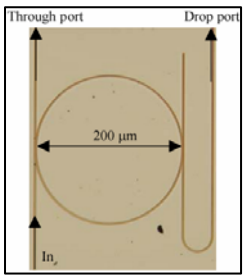
HIGH-SPEED RECEIVER

IBM

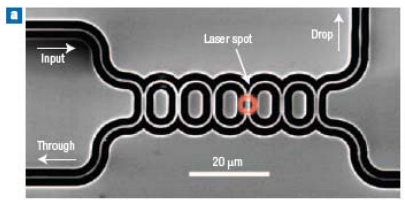


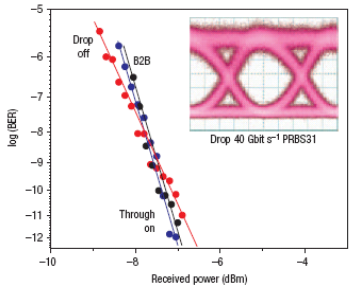
BROADBAND MULTI-λ ROUTER SWITCH

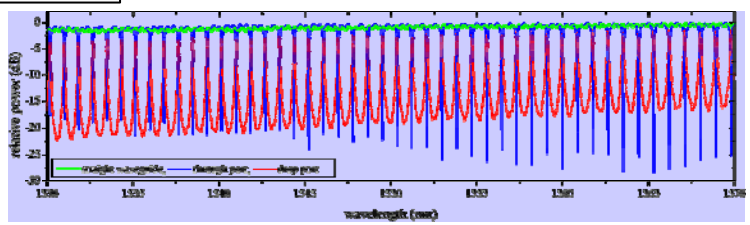
Cornell/ Columbia

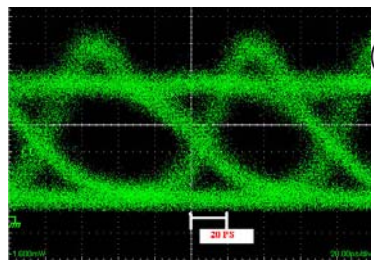


IBM

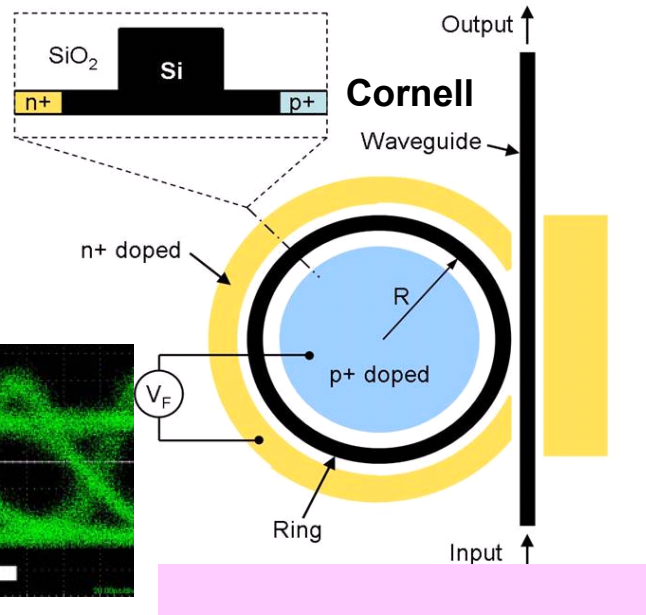






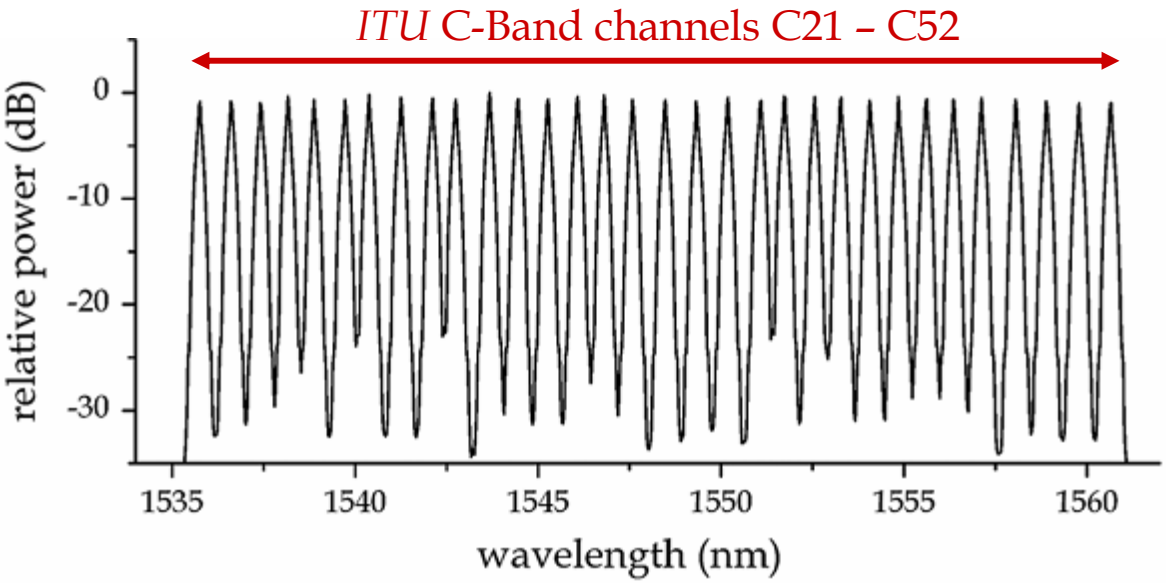


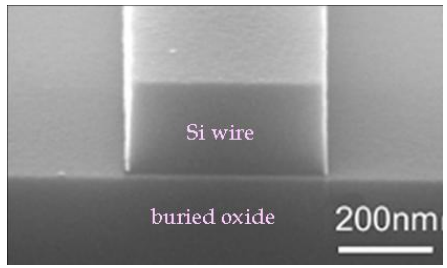
HIGH-SPEED MODULATOR



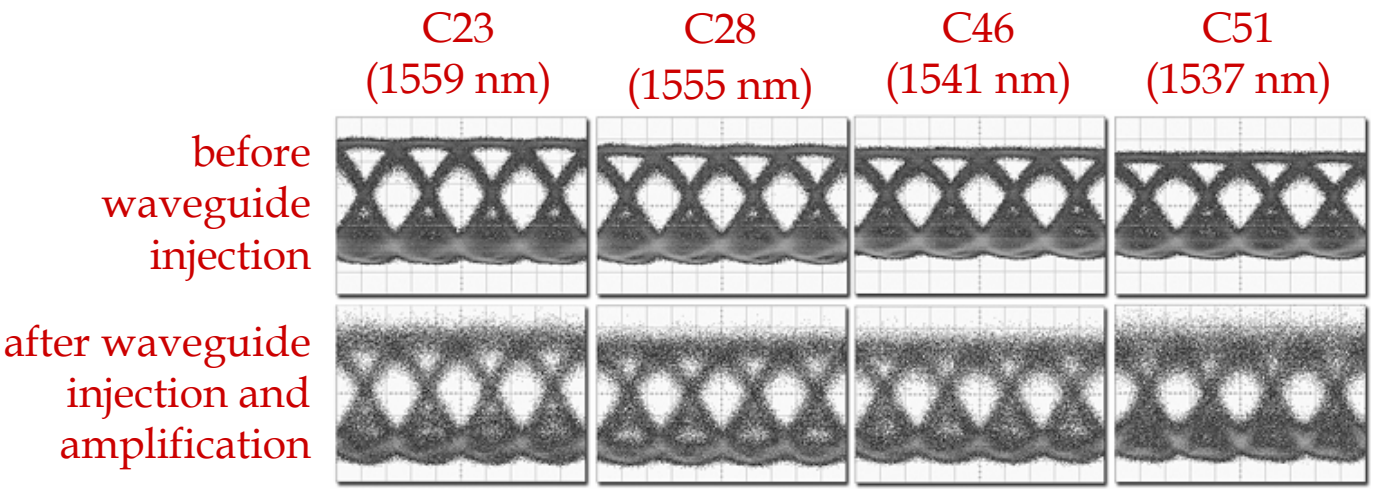
Silicon Photonic Nanowire Waveguide Broadband Links

1.28-Tb/s Results

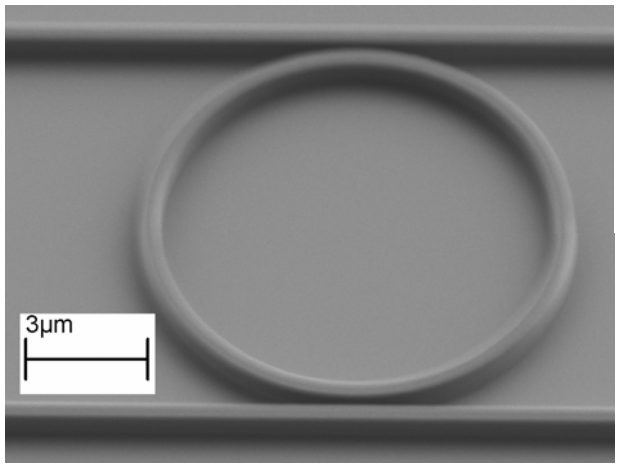


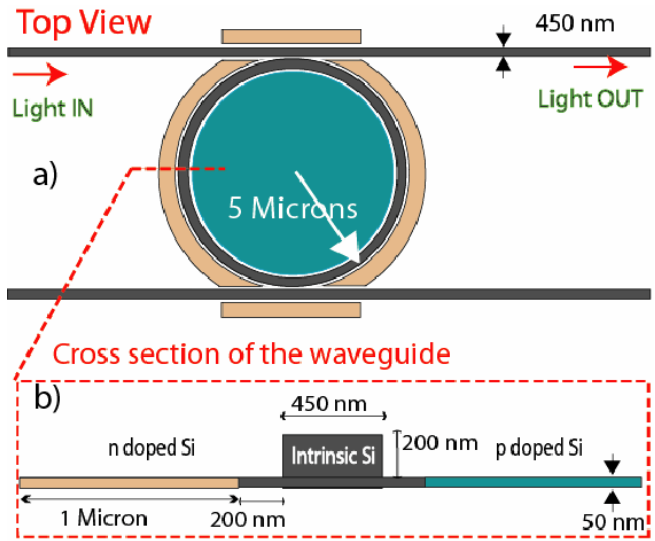


- **40 Gb/s per channel**
- **32 channels (100-GHz spacing)**
- **1.28 Tb/s data stream**



Resonant Silicon Electrooptic Modulators





- Ultra compact: Scalable to ~1.5 micron radius.
- Ultra low power: per bit energy ~ 100 fJ
- Low insertion loss : <0.1 dB

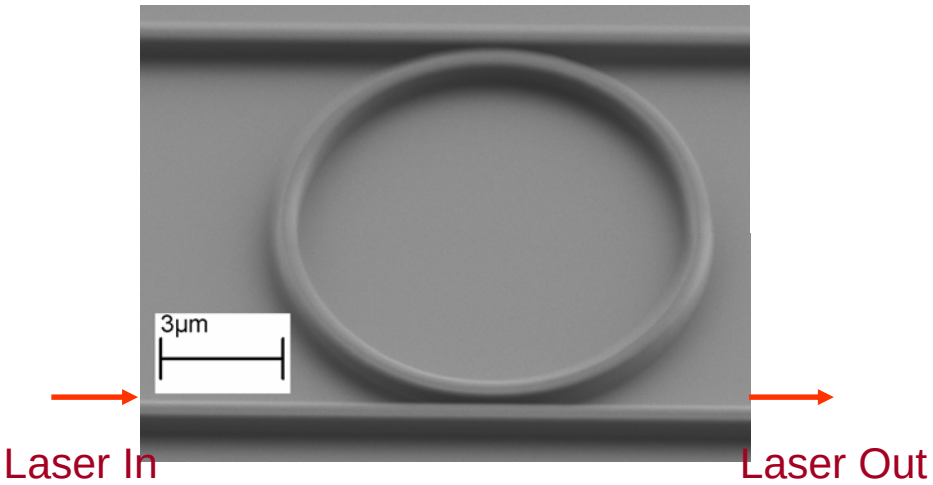
Small Foot print

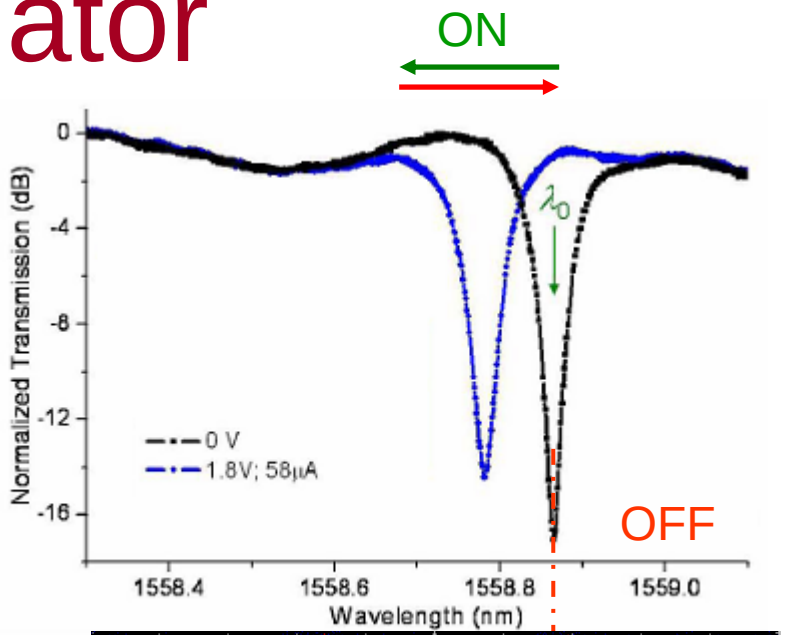
Low Electrical Power

Low Optical Power

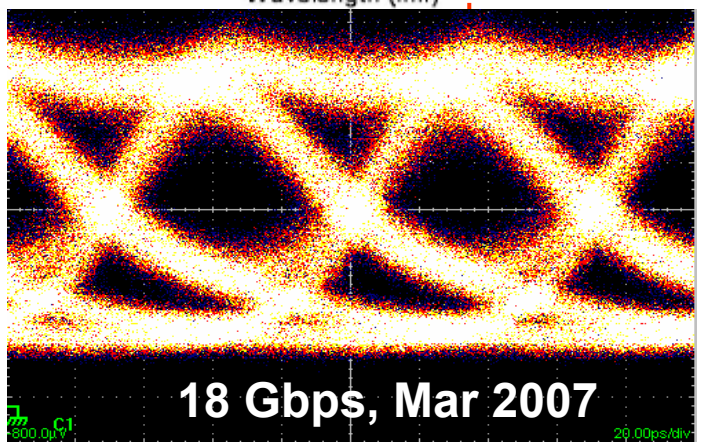
Here, we show operation of resonant modulators over a wide temperature range.

Microring Silicon Electrooptic Modulator



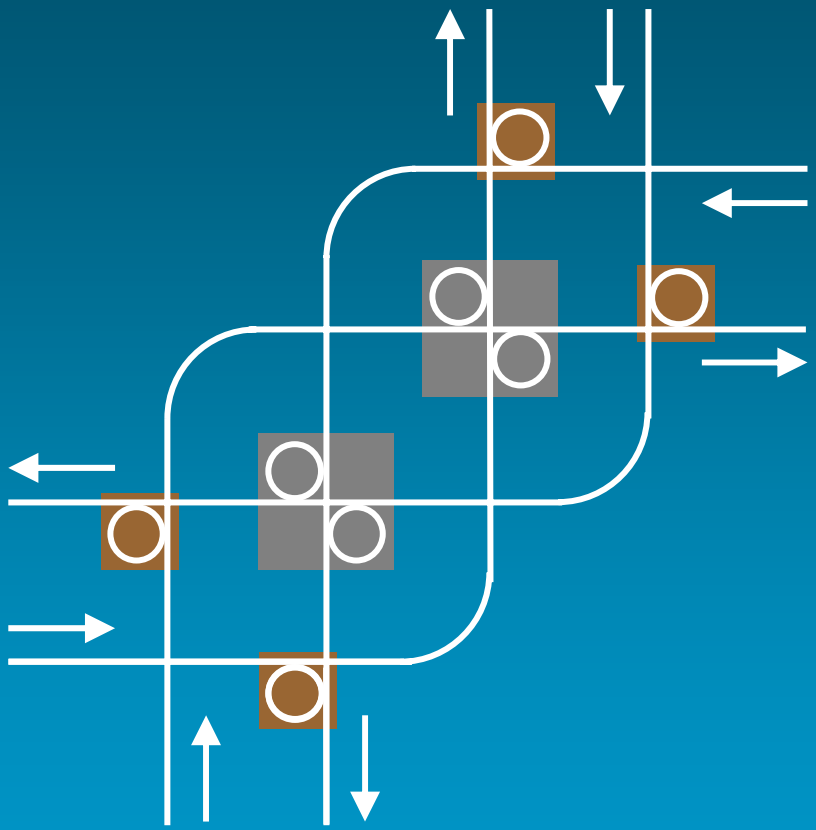


- NRZ Modulation at 18 Gbit/s
- ~10 dB Extinction Ratio

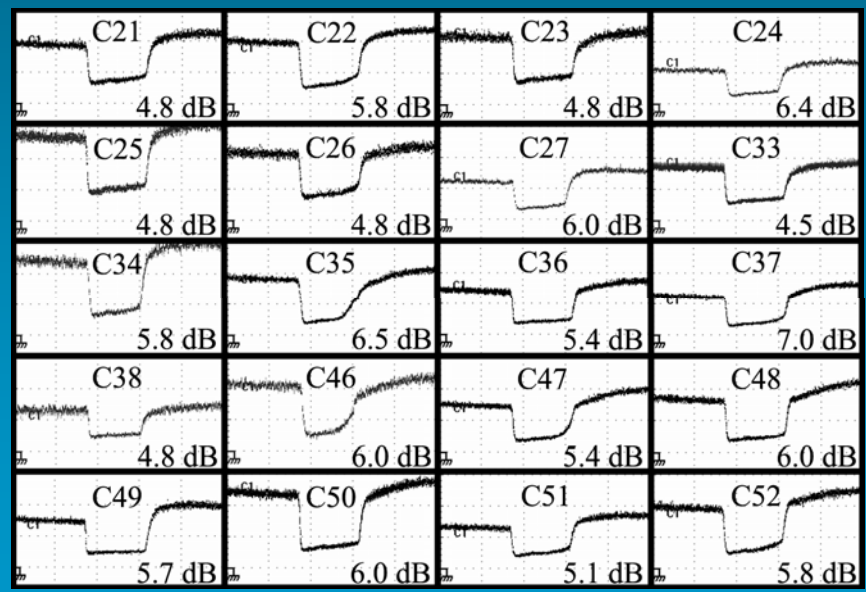


S. Manipatruni, M. Lipson et al LEOS 2007

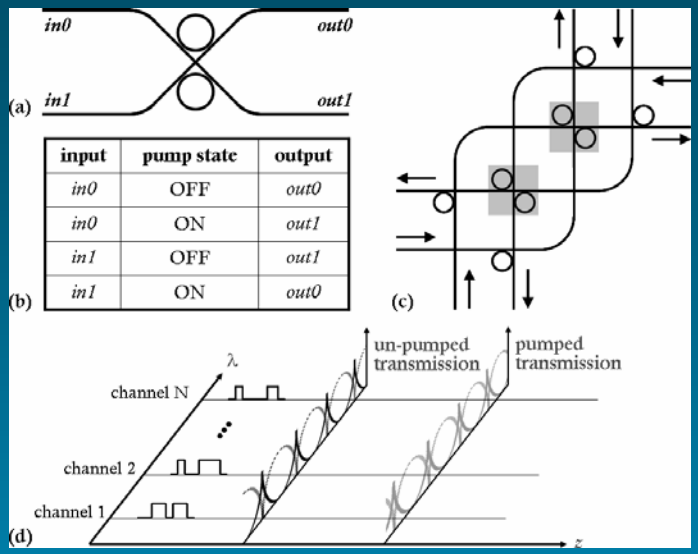
Multi-wavelength silicon photonic routers

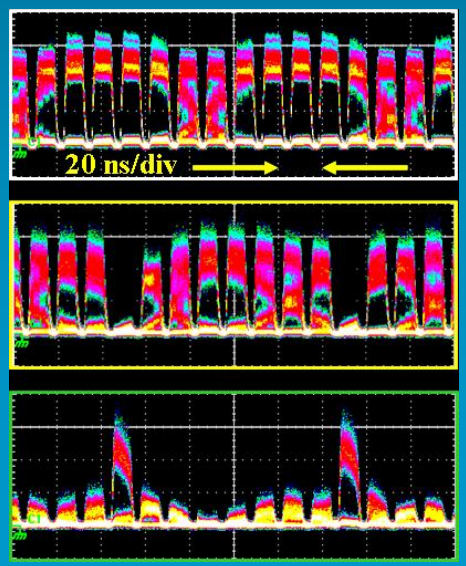


[A. Biberman, *OFC*, OTuF6 (2008)]

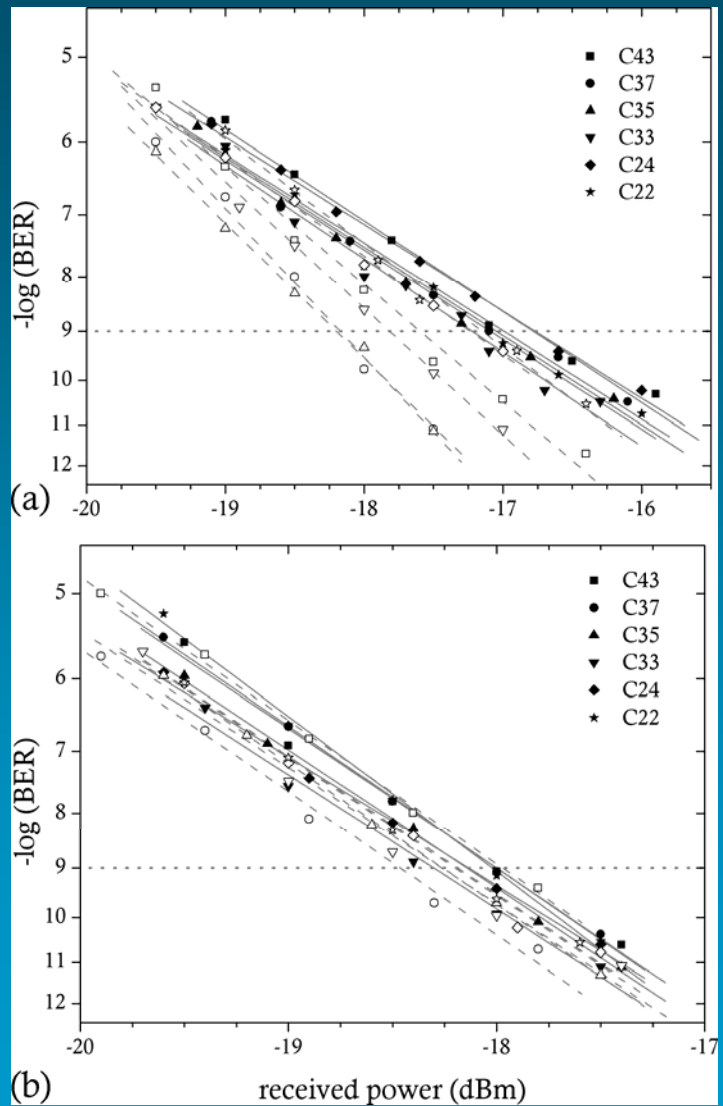


Recent 2x2 and 4-port router

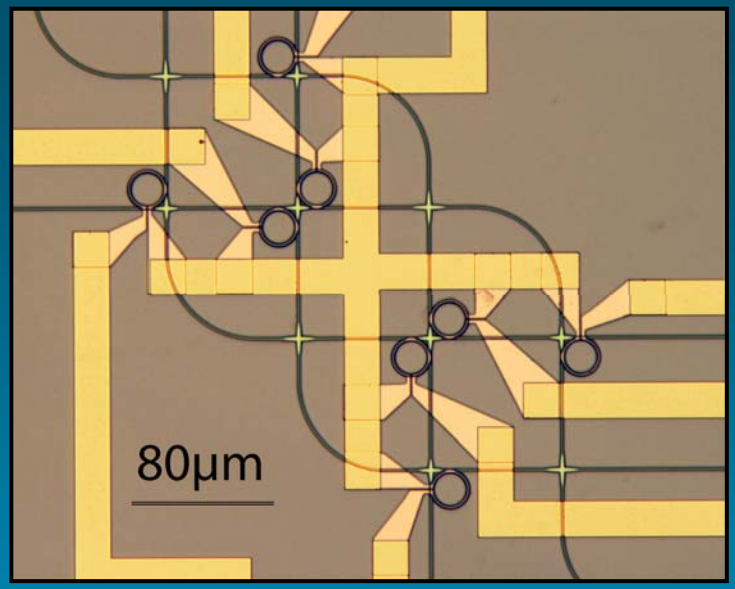




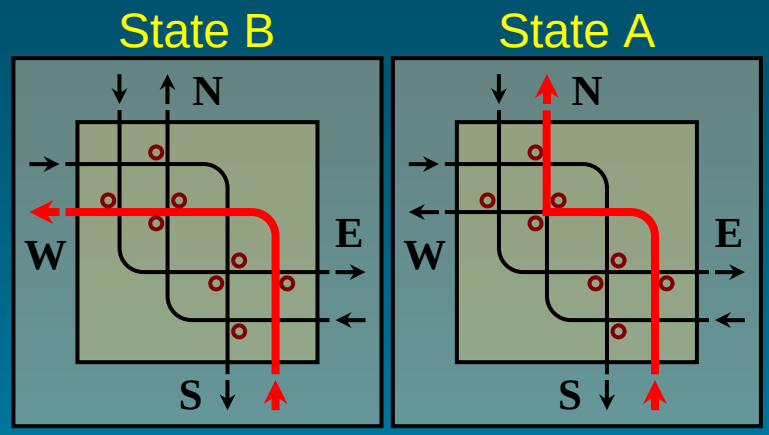
2x2 multi-wavelength bar and cross BER



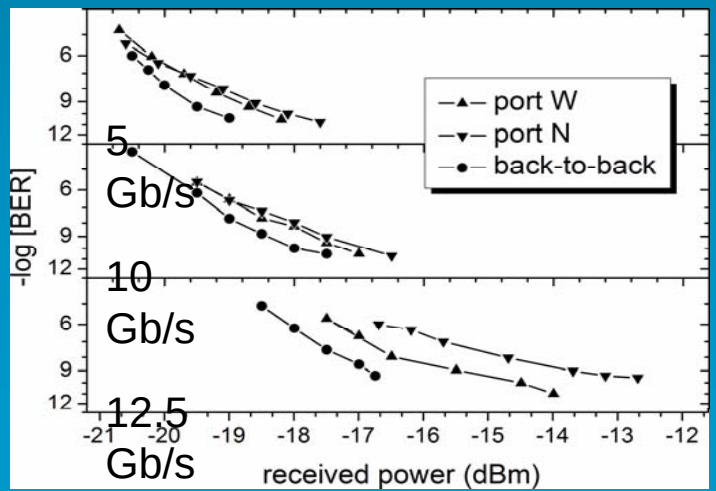
4x4 Non-Blocking Router



Microscope image



Schematic with experimental paths highlighted



NoC + Memory Simulator

Network View

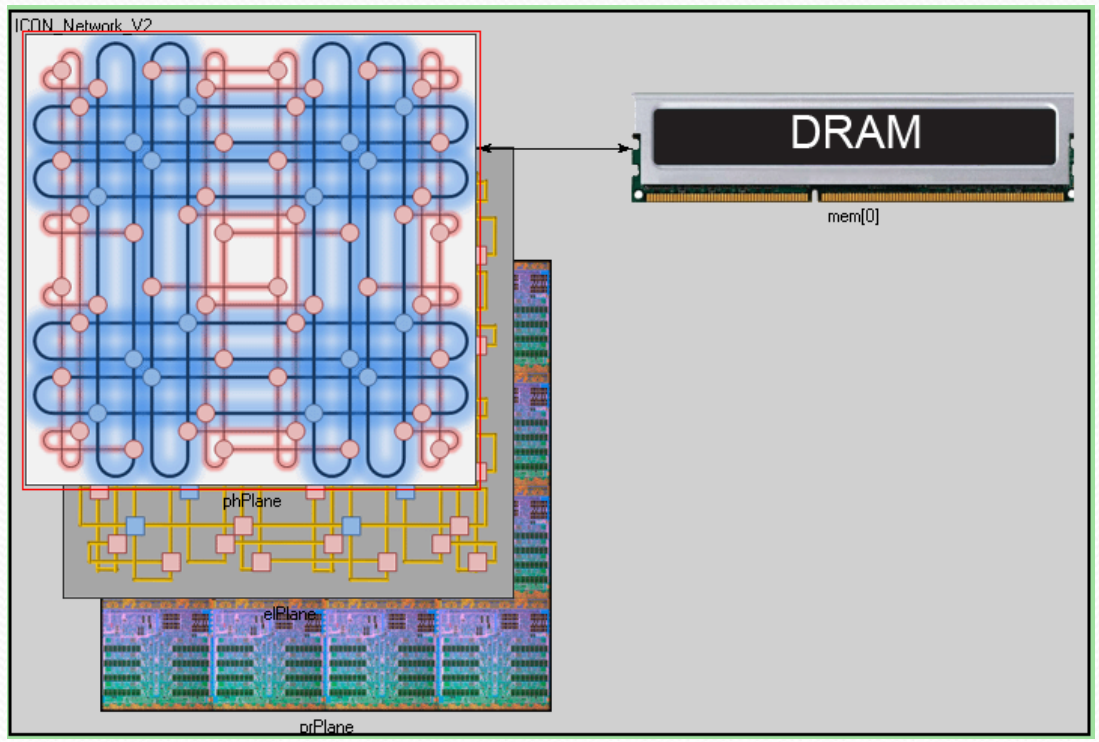
OMNeT++ Simulation Environment

NoC (3 planes)

- •Photonic Plane
- •Electronic Plane
- •Processing Element Plane

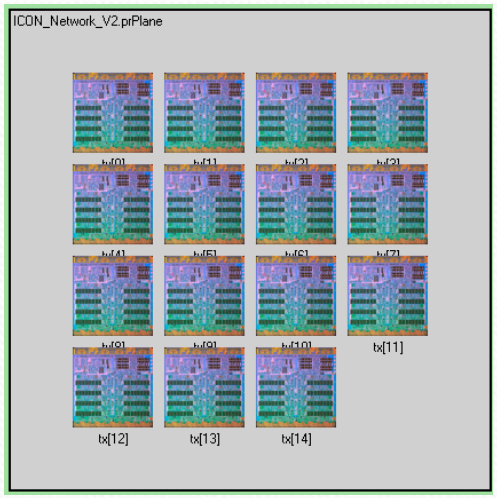
Memory

- •Scalable # of Banks
- •Scalable Bank Size
- •Direct Connection to Supercore L2 Cache Via Photonic Plane

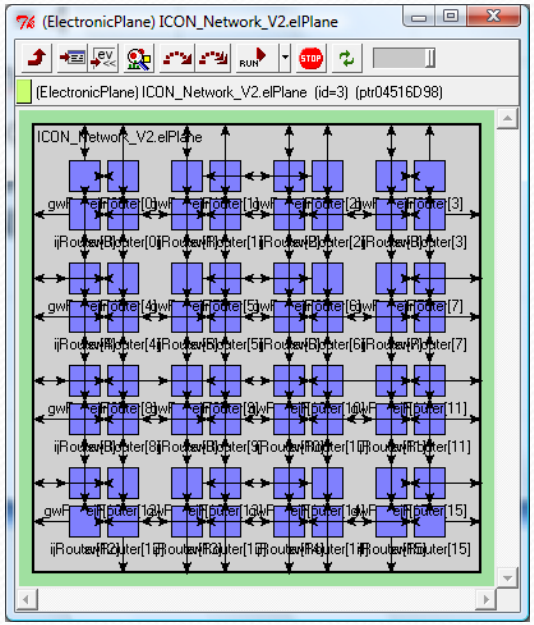


NoC + Memory Simulator

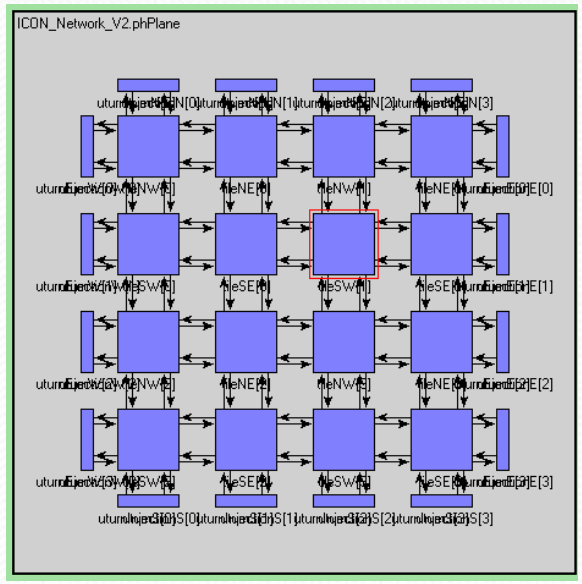
Processing Element Plane



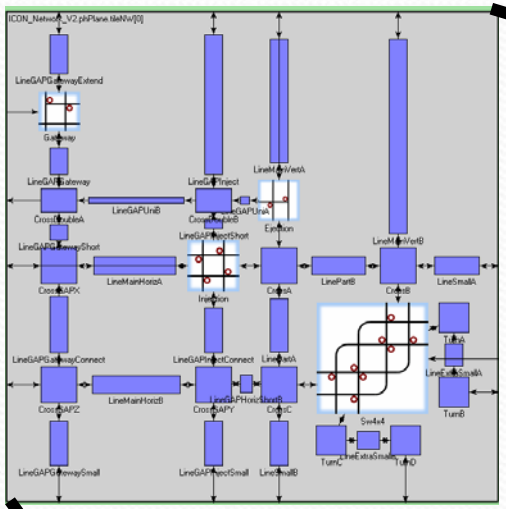
Electronic Plane



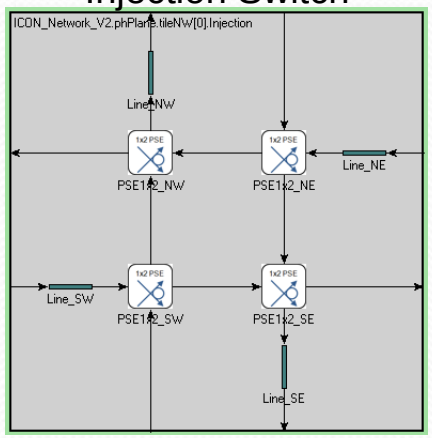
Photonic Plane



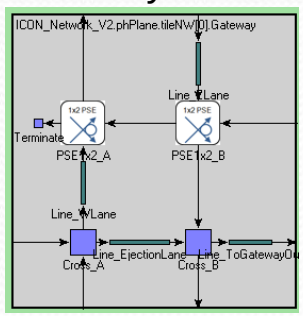
NoC + Memory Simulator: Photonic Plane -- Tile



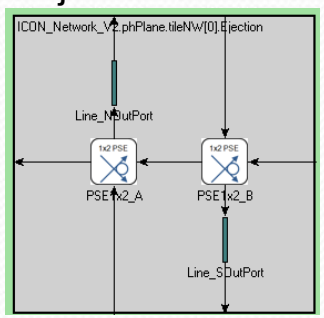
Injection Switch



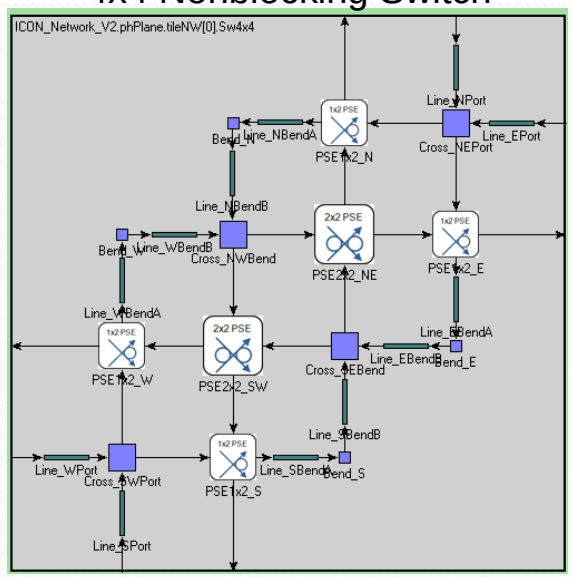
Gateway Switch



Ejection Switch



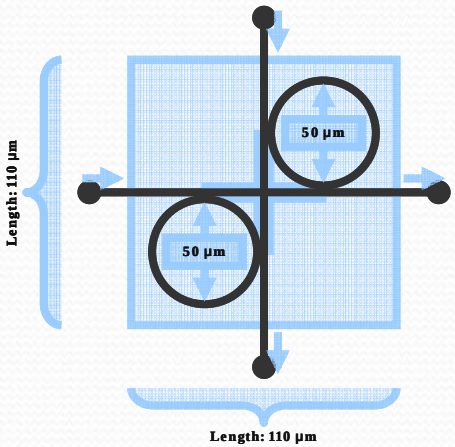
4x4 Nonblocking Switch



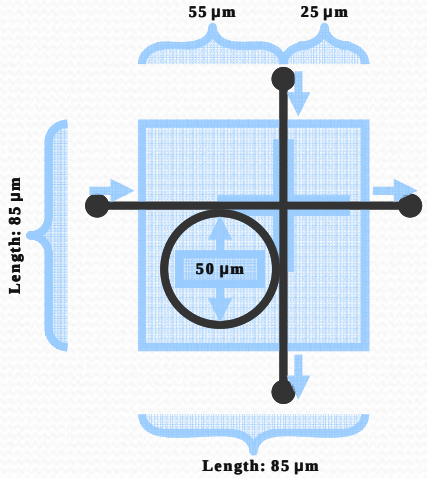
Photonic Plane – Building Blocks

- Switching Elements

2x2 PSE

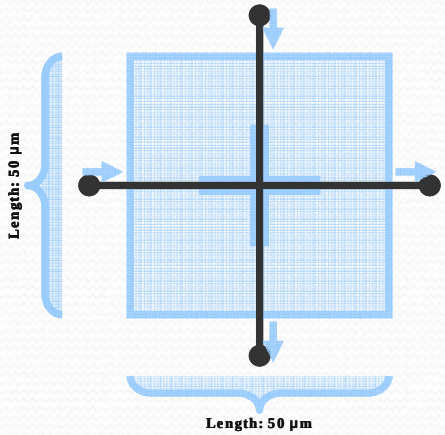


1x2 PSE

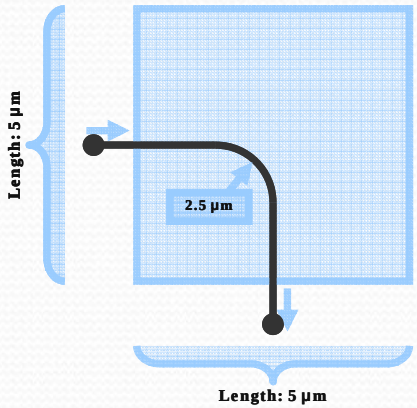
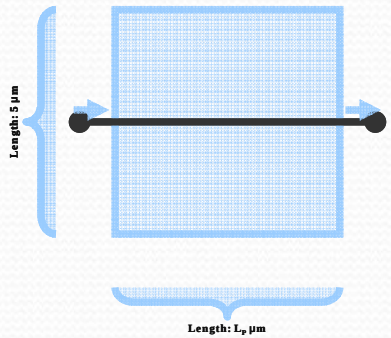


- Passive Components

Crossing



Bending



Propagation